JF24C firmware control

JF24C & MCU control interface

Packet definition and FIFO point

JF24C system initiation flow chart

JF24C TX state flow chart

JF24C RX state flow chart

Introduction of JF24C register setting

Recommended register setting

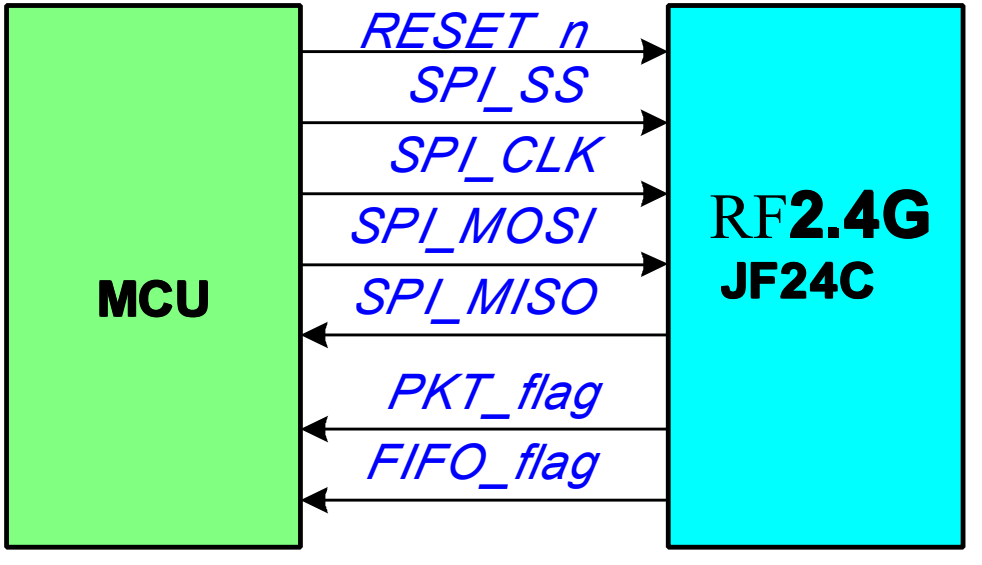
How to read RSSI value from JF24C?

Question and answer

JF24C & MCU control interface

Digital Interface

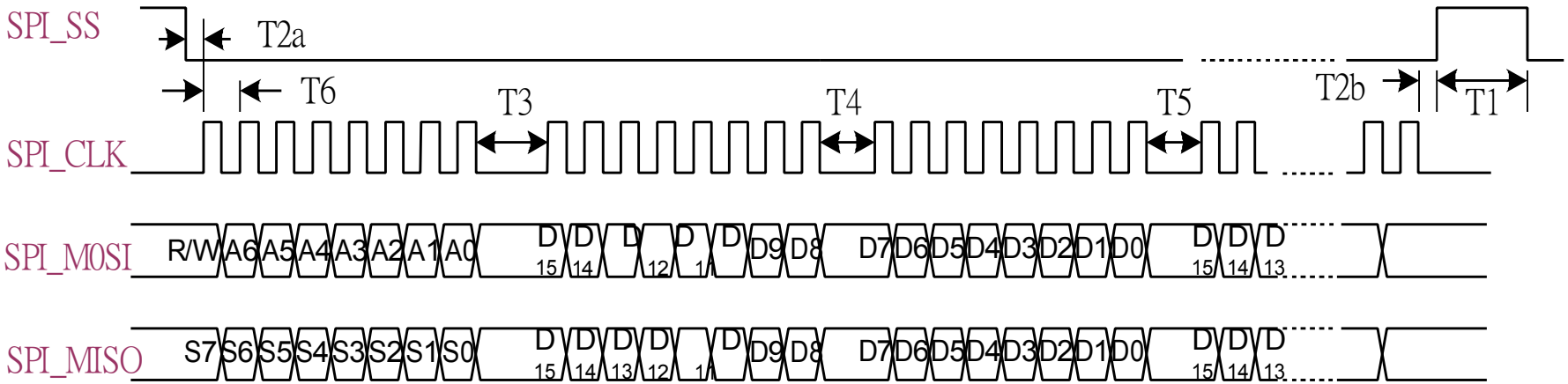
- JF24C provides a simple interface for application MCU, consisting of SPI interface plus two handshake signals.
- JF24C SPI supports slave mode only. It supports two SPI standa formats (CKPHA =0 and CKPHA=1). Please refer to JF24C datasheet for detailed description of CKPHA and the associated data formats.



JF24C & MCU control interface

SPI Timing Diagram

- Here is the description of the SPI signals timing diagram. For illustration purpose, CKPHA=0 is shown (SPI_MOSI data clocked in on rising edge of SPI_CLK).



Pin	Description
SPI_CLK	SPI clock input
SPI_SS	SPI slave select input
SPI_MOSI	SPI data in
SPI_MISO	SPI data out
PKT_flag	Packet TX/RX flag
FIFO_flag	FIFO full/empty flag
RESET_n	Reset input, active low

Name	Min.	Typ.	Max.	Description
T1	250ns			Interval between two SPI accesses
T2a, T2b	41.4ns			Relationship between SPI_SS & SPI_CLK
T3	* (1)			Interval time between two address and data
T4	* (2)			Interval time between high byte and low byte data
T5	* (3)			Interval time between two register data
T6	83ns			SPI_CLK period

Notes:

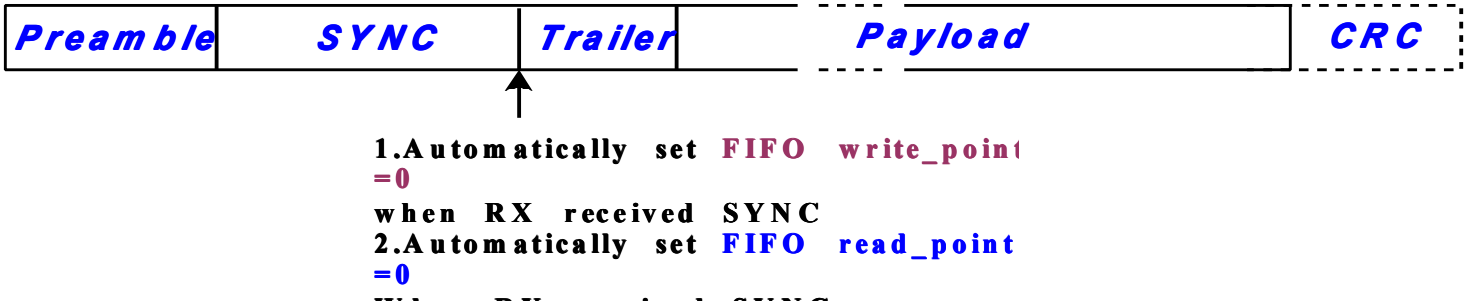
(1) If reading register 0x00~0x1f, at least 3us wait time is required, it is used to get register(0x00~0x1f) value after framer decoded the address SPI required. If reading FIFO data, at least 450ns wait time is required, it is used to get correct FIFO read point. Otherwise, T3min = 41.5ns

(2). If reading FIFO data, at least 450ns wait time is required, it is used to get correct FIFO read point. Otherwise, T4min = 41.5ns.

(3) If writing register 0x00~0x1f, at least 3us wait time is required, it is used to program register(0x00~0x1f) for internal BuleRF interface Dbus If read FIFO data, at least 450ns wait time is required. Otherwise, T5min = 41.5ns.

Packet definition and FIFO point

Packet Definition and FIFO Point Clear



Preamble: 1~8 bytes programmable.

SYNC: 32/48/64 bits programmable as device syncword

Trailer: 4~18bits programmable

Payload: TX/RX data, there are 4 data types: raw data, 8_10 bits, Manchester, and interleave with FEC option.

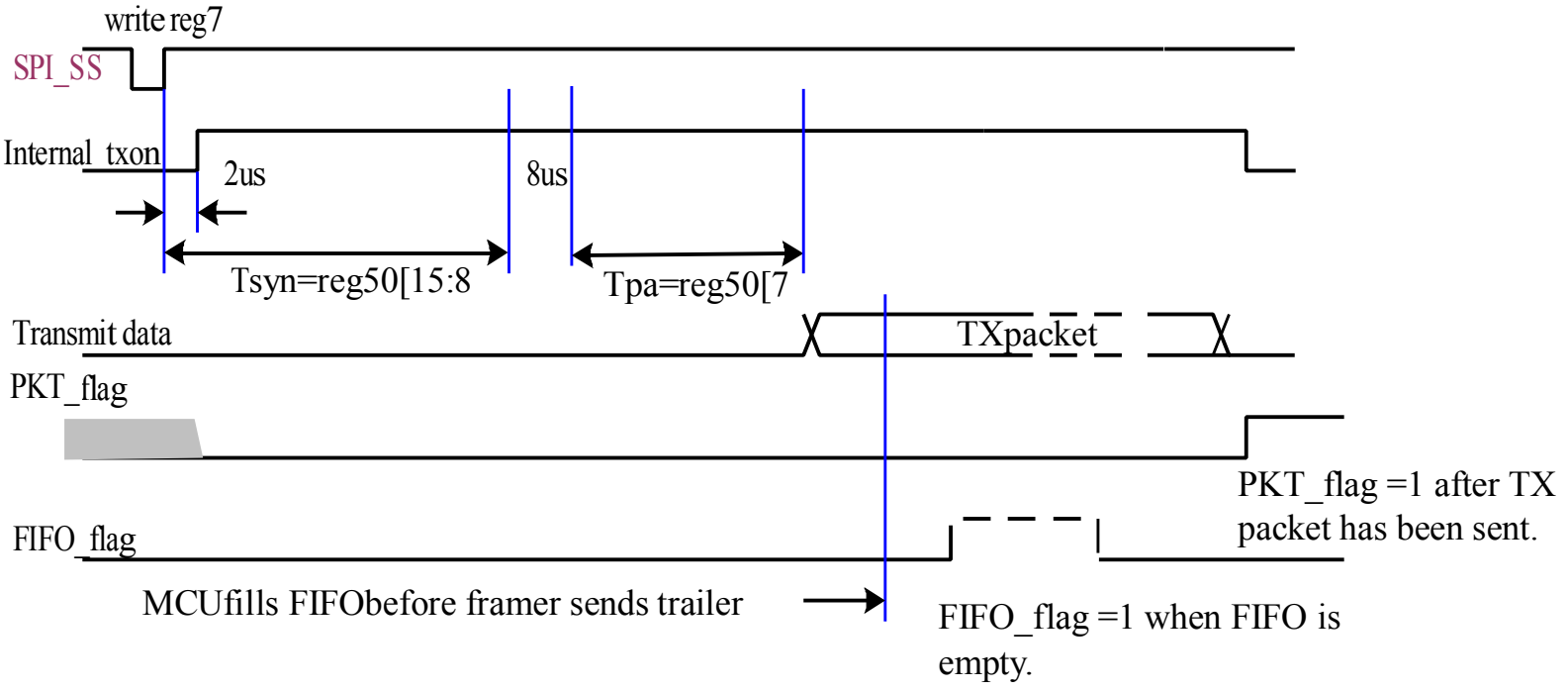
CRC: 16bit CRC is optional

Note: For transmit, it is required to clear FIFO write point before application writes in data via access reg82[15].

JF24C TX/RX timing diagram

- Framer detect packet length

TX

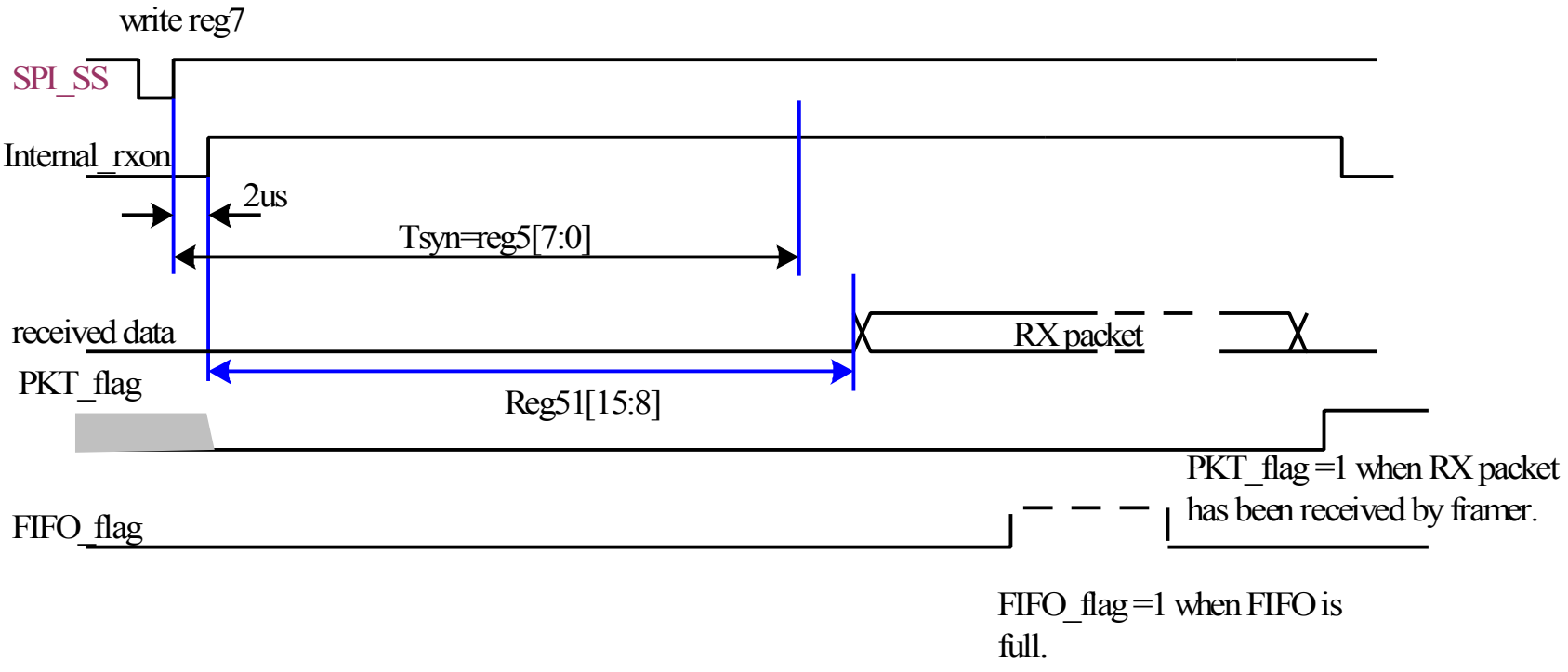


TX timing diagram when PKT_flag and FIFO_flag are high active
(framer detect packet length)

JF24C TX/RX timing diagram

- Framer detect packet length

RX

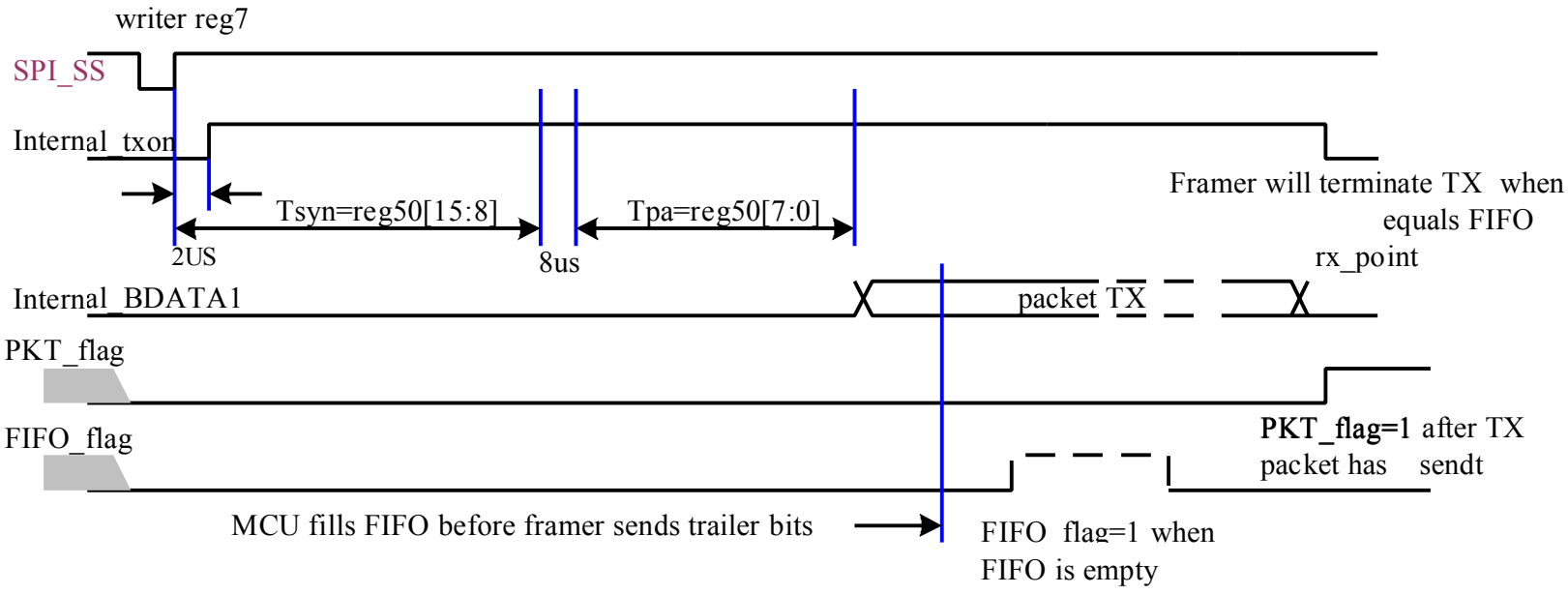


RX timing diagram when PKT_flag and FIFO_flag are high active
(framer handle packet length)

JF24C TX/RX timing diagram

- MCU handle packet length

TX

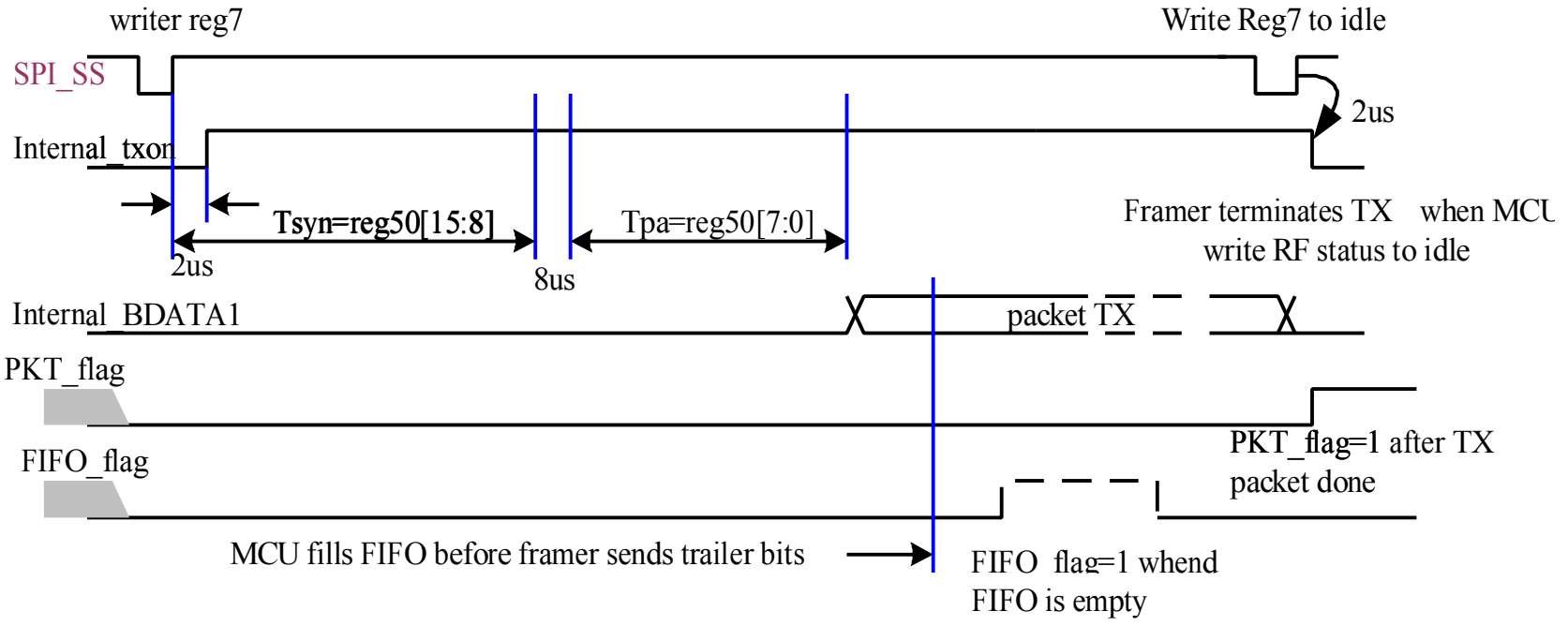


TX timing diagram when PKT_flag and FIFO_flag are high active
(MCU handle packet length, framer determinate TX)

JF24C TX/RX timing diagram

- MCU handle packet length

TX

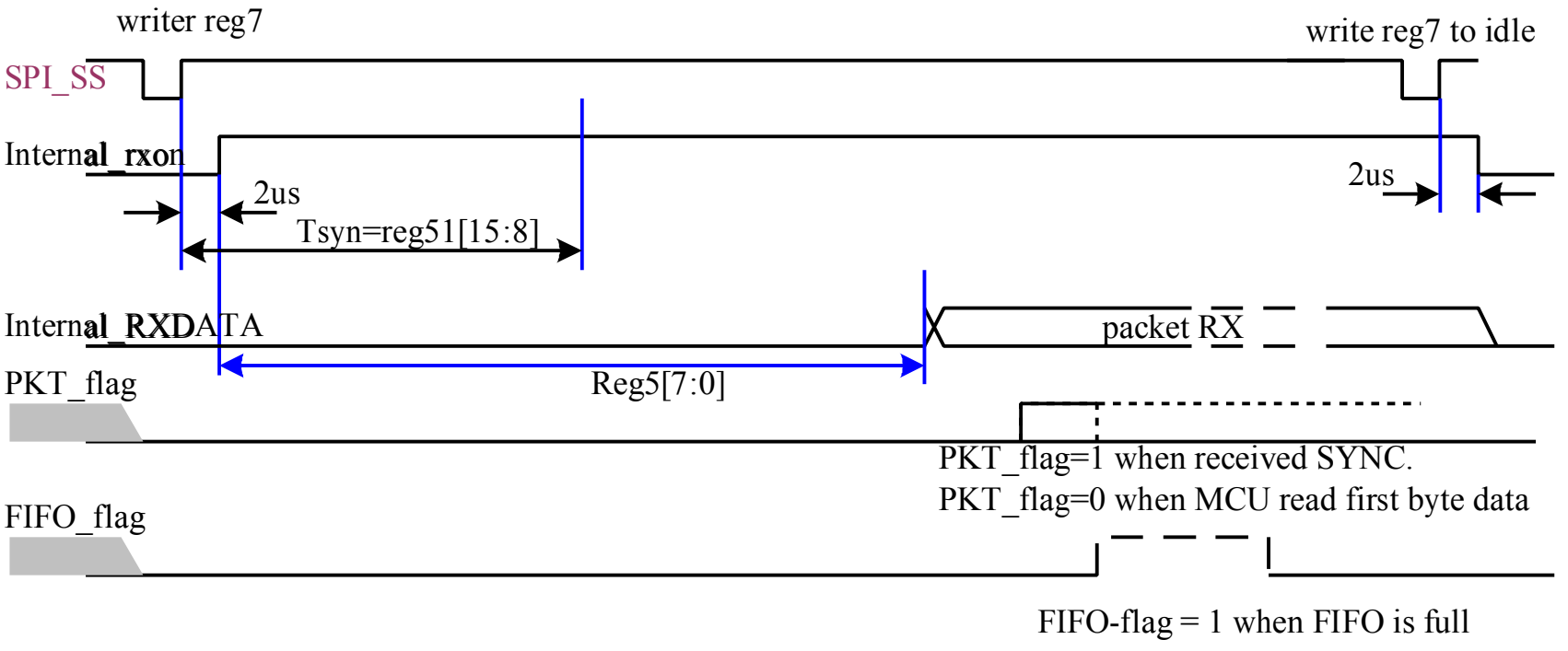


TX timing diagram when PKT_flag and FIFO_flag are high active
(MCU handle packet length, framer doesn't detect FIFO W/R point)

JF24C TX/RX timing diagram

- MCU handle packet length

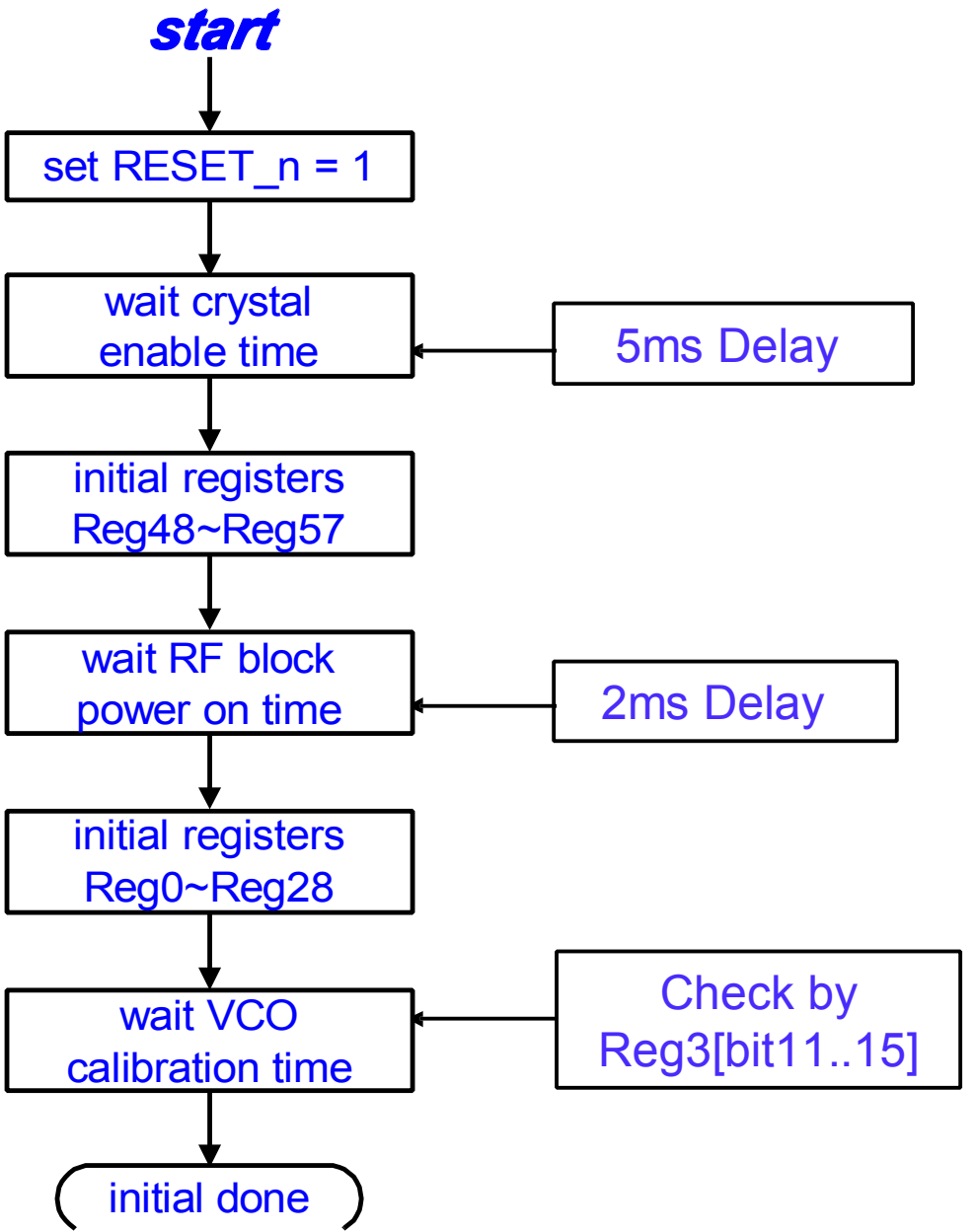
RX



RX timing diagram when PKT_flag and FIFO_flag are high active
(MCU handle packet length)

JF24C system initiation flow chart

Initial flow

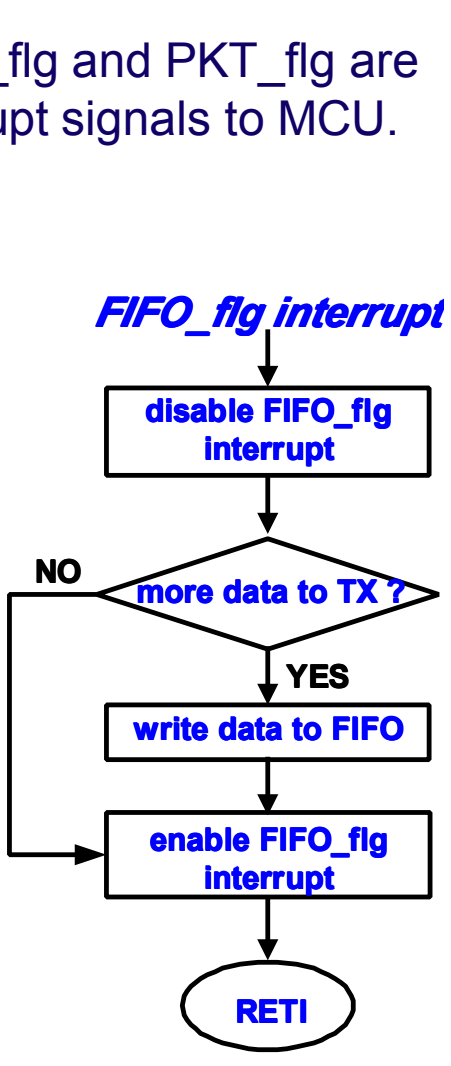


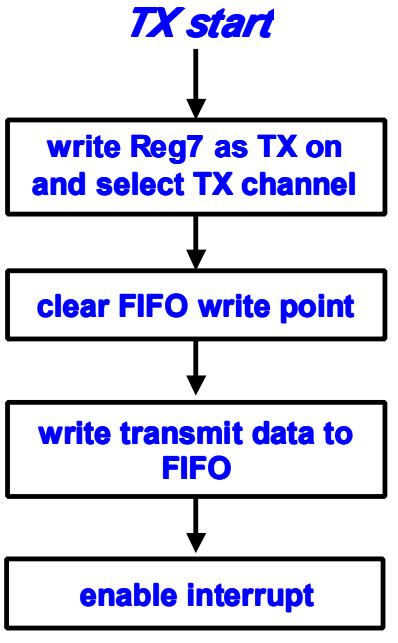
JF24CState Flow Chart

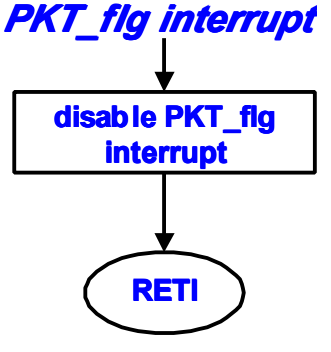
- Framer detect packet length

TX flow

FIFO_flg and PKT_flg are interrupt signals to MCU.





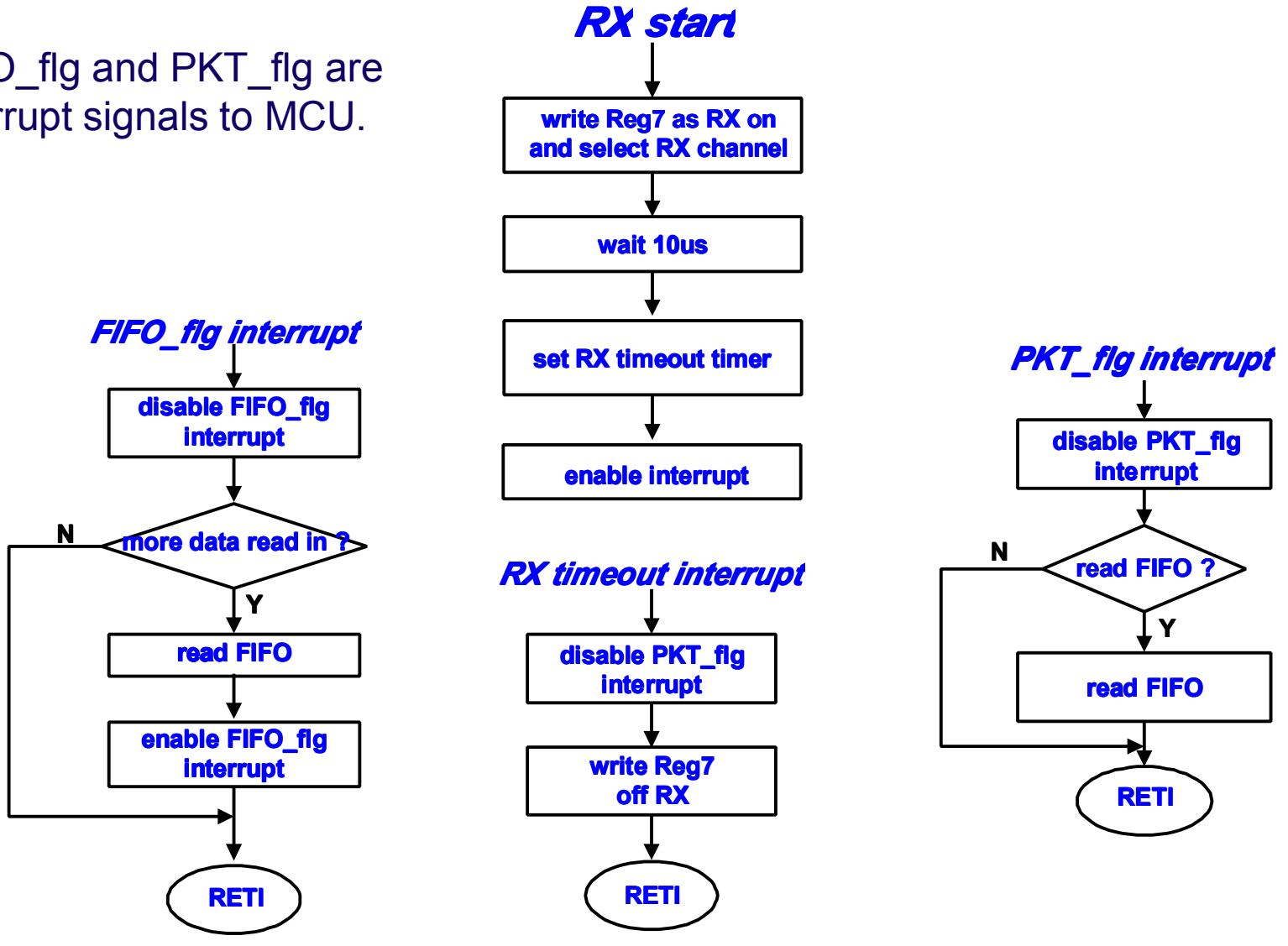


JF24CState Flow Chart

- Framer detect packet length

RX flow

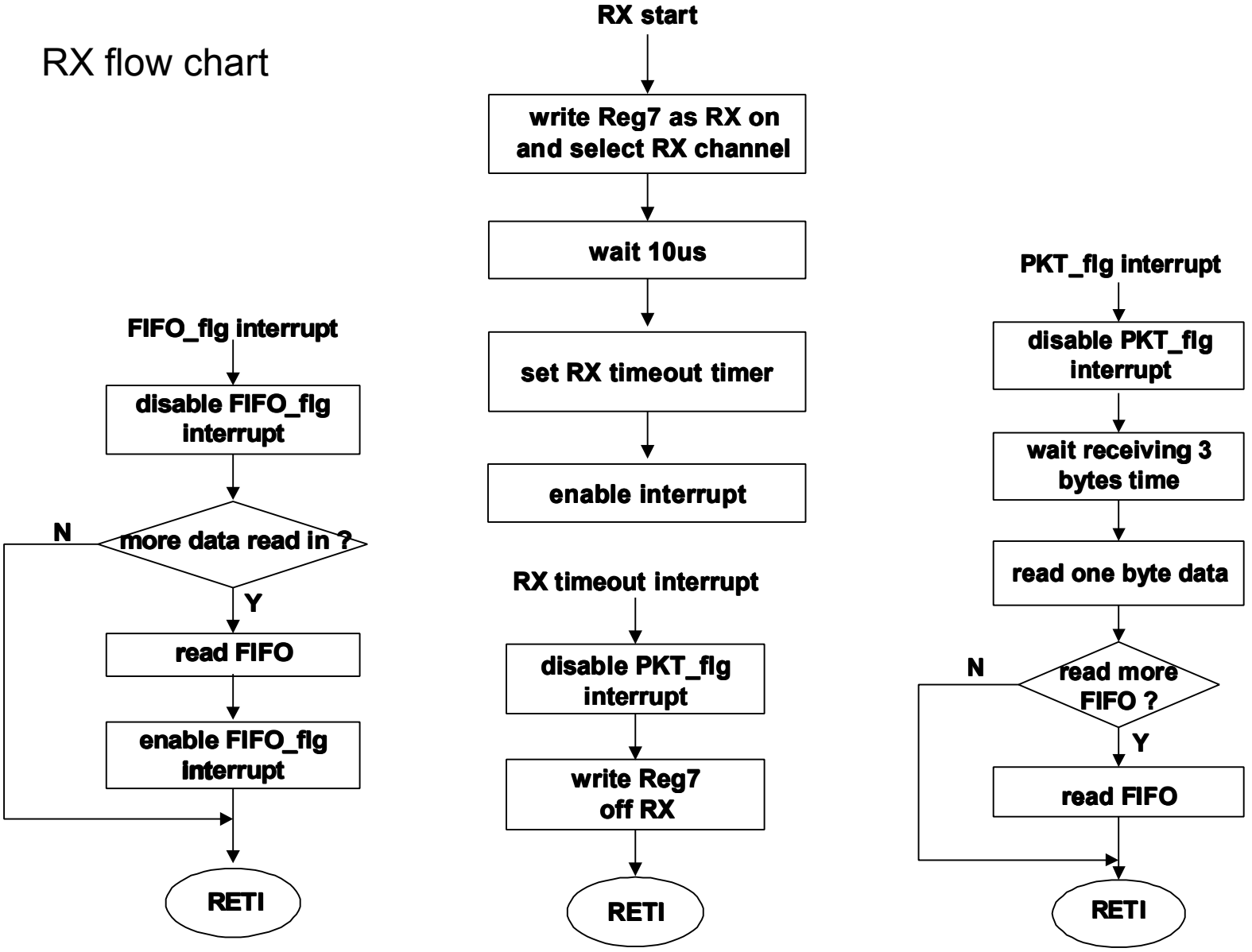
FIFO_flg and PKT_flg are interrupt signals to MCU.



JF24C State Flow Chart

- MCU handle packet length

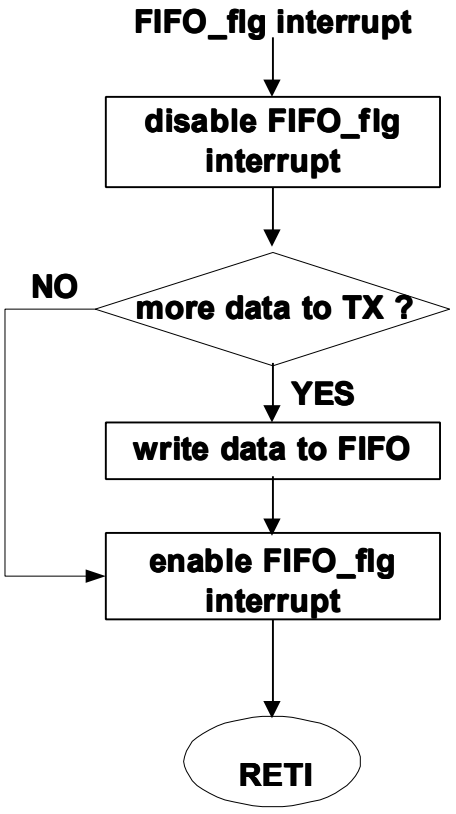
RX flow chart

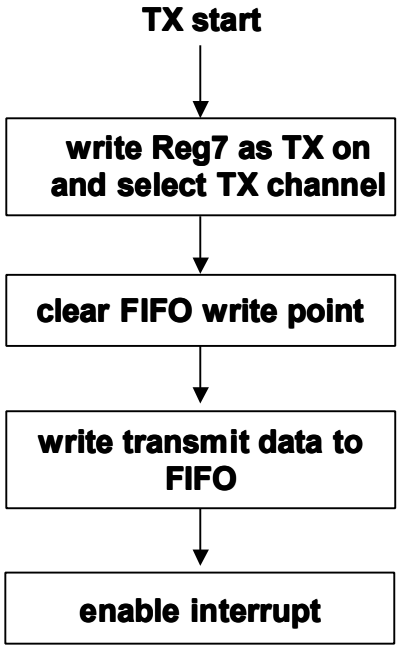


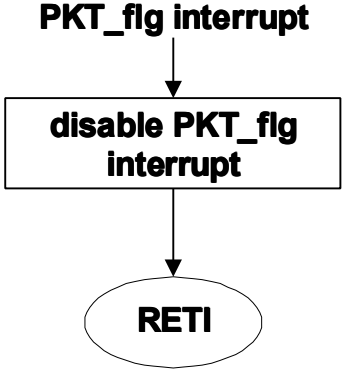
JF24C State Flow Chart

- MCU handle packet length

TX flow chart
(framer detect FIFO TX/RX point)



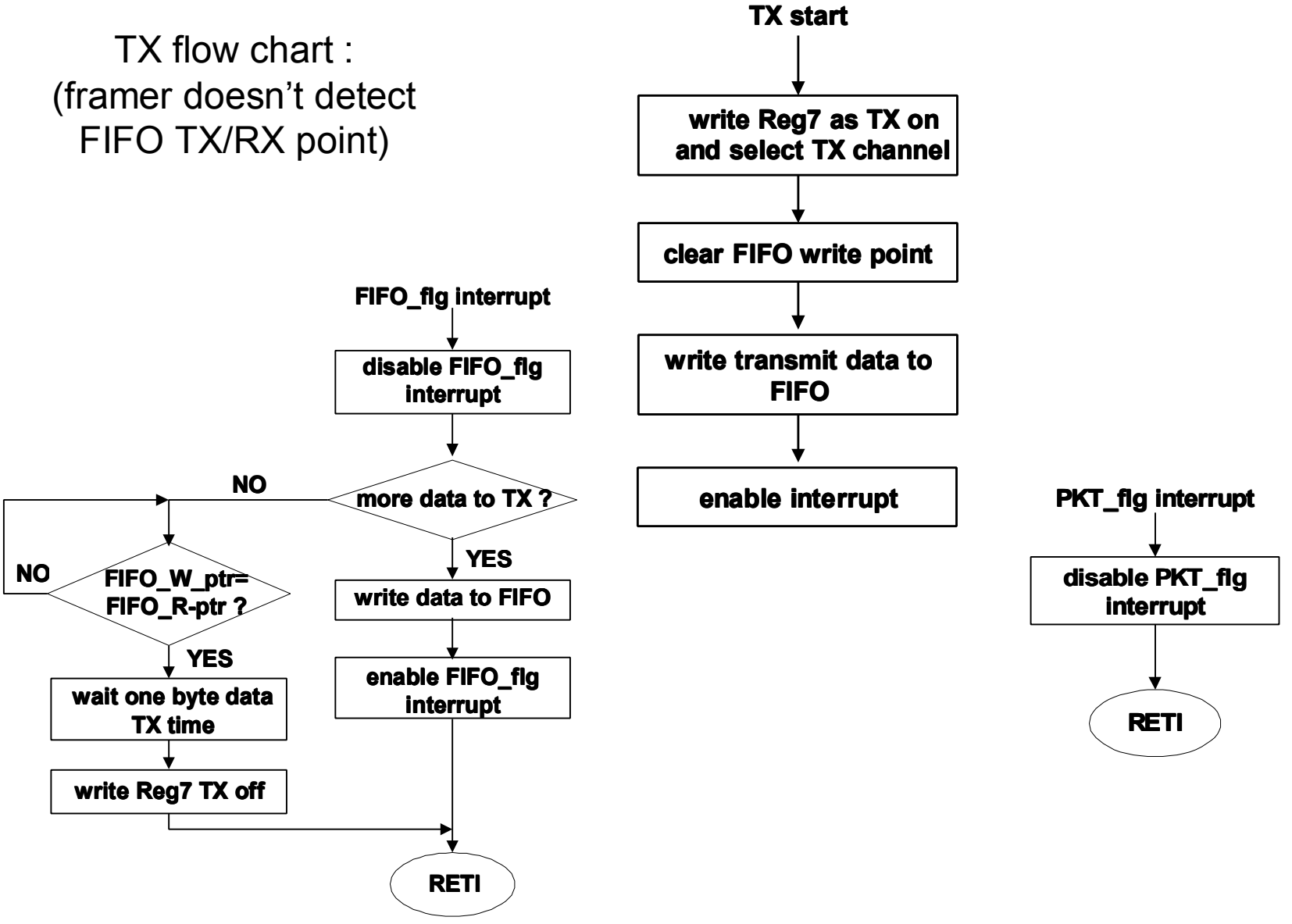




JF24C State Flow Chart

- MCU handle packet length

TX flow chart :
(framer doesn't detect
FIFO TX/RX point)



Introduction of JF24C register setting

TX/RX Status (Read only) – Register 3

Bit No.	Bit Name	Description
15 – 11	BLUE_RF_STATE[4:0]	Show up the status of BlueRF finite state machine.
10	RC_FIN	RC finish status from RC CALC circuit.
9 - 6	VCO_CAL[3:0]	Indicate the current VCO frequency band setting after automatic calibration.
5	VCO_CAL_ERROR	An error flag indicates that no proper VCO curve can be found.
4	RF_SYNTH_LOCK	Indicate the lock status of RF synthesizer.
3 - 0	TEMP_SENSOR[3:0]	Indicate the current temperature range.

BLUE_RF_STATE

BLUE_RF_STATE [4:0]	STATE
00000	Off
00001	PwrOnWaitXTL
00010	HoldXTL
00011	Idle
00100	Sleep
00101	SleepWaitXTL
00110	VCO_Sel
00111	VCO_Wait
01000	RXPLLWait1
01001	RXPLLWait2

BLUE_RF_STATE [4:0]	STATE
01010	RXWideFilt
01011	RXNarrowFilt
01111	VCO_PwrOnWait
10000	WaitDataSync1
10001	WaitDataSync2
10010	DataSync
10011	EnblePA1
10100	EnblePA2
10101	TXData
10110	DisablePA1
10111	DisablePA2
11000	DisablePA3

Introduction of JF24C register setting

RF TX Control (Write/Read) – Register 4 (Default = 0x3CD0)

Bit No.	Bit Name	Description
15 -14	RSSI_GN_ADJ[1:0]	RSSI control signal.
13-10	TXDAC_DC[3:0]	Set 4-bit value for TXDAC DC voltage level.
9	RSSI_DIS	"1": disable RSSI feature.
8	reserved	
7 – 3	TXDAC_GAIN[4:0]	Set 5-bit gain value for TXDAC.
2 -0	BG_TBIT[2:0]	Set 3-bit test-mode control for BandGap Reference.

TX Coefficient/RSSI Value (Read only) – Register 6

Bit No.	Bit Name	Description
15 – 10	RAW_RSSI[5:0]	Indicate 4-bit raw RSSI values from analog circuit; for internal debugging purpose.
9	AGC	Indicate the current 1-bit AGC value. (See also Registers 14 and 17.)
8	RSSI_VALID	Indicate if the current RSSI value (bit 3-0 of this register) is valid.
7 -0	RSSI[7:0]	Indicate the current 8-bit RSSI values.

Introduction of JF24Cregister setting

RF Synthesizer / TX-RX Control (Write/Read) – Register 7 (Default = 0x0030)

Bit No.	Bit Name	Description
15 - 14	Reserved	
13 - 9	SWALLOW [4:0]	5-Bits Synthesizer Swallow counter. When the RF_PLL_DIRECT is set to "1", the synthesizer will be programmed directly with Register7[13:9] and Register7[6:0]. The frequency of synthesizer will not be programmed as f = 2402+ PLL_CH_NO again.
8	DBUS_TX_EN	Enable the Transmit Sequence for state machine control
7	DBUS_RX_EN	Enable the Receive Sequence for state machine control. Note that DBUS_TX_EN and DBUS_RX_EN cannot be "HIGH" at the same time;otherwise, the configuration to Thunder cannot work.
6 - 0	RF_PLL_CH_NO [6:0] /RF_PLL[6:0]	7 bits stand for the Bluetooth RF channels. The channel frequency will be: f = 2402+ PLL_CH_NO. When the RF_PLL_DIRECT is set to "1", the synthesizer will be programmed directly with Register7 [13-9] and Register7[6:0] Register7[6:0] are used as 7-bits Synthesizer Program counter The frequency of synthesizer will not be programmed as f = 2402+PLL_CH_NO again.

Introduction of JF24C register setting

RFIC Control (Write/Read) – Register 9 (Default = 0x3003)

Bit No.	Bit Name	Description
15--12	Reserved	
11-7	PA_GN[4:0]	5-bit transmit power amplifier gain setting
6	TR_SW_POLARITY	When “0”, the default polarity of TR_SW is selected (TR_SW:”0” is for transmitting; “1’ is for receiving); “1” the polarity of TR_SW is Inverse.
5	APLL_VT_SENSE	APLL VT sense bit.
4	APLL_VT_FORCE	APLL VT force bit.
3	APLL_BP	Analog PLL Bypass mode. When “1”, Fout = Fin.
2	APLL_PDN	Analog PLL power-down mode. When “1”, APLL is power-off .
1	BRCLK_SEL	The selection pin for the BRCLK. If BRCLK_SEL = “1”, BRCLK = crystal_out or If BRCLK_SEL = “0”, BRCLK = TXCLK(1MHz). (default = “1”)
0	BRCLKEN	The output of BlueRF interface BRCLK works when BRCLKEN is high.(default = “1”)

Introduction of JF24C register setting

AMS TEST Control (Write/Read) – Register 10 (Default = 0x0004)

Bit No.	Bit Name	Description
15	ENTER_SLEEP	When "1" is given, chip will enter into sleep mode to save power.
14	AMS_TST_ENB	When "1" is given, enable the AMS test mode and bypass BlueRF finite state machine.
12-13	AMS_TST_MD_SEL	00 : Normal operation mode, 01 : Enable the test for the digital to analog converter of the transmit I channel. 10 : Enable the test for the digital to analog converter of the transmit Q channel. 11 : Enable the test for the analog to digital converter of the RSSI.
11	TXDAC_MOD_MON	Enable DAC output monitor enable
10	BPF_TST_PD	When "1", indicate to power down the band pass filter during AMS_TST_ENB = "1".
9 – 8	reserved	
7	Ext_pa_sel	0: RXDATA=EXT_PA_CTRLo, Test1=EXT_TR_SW(0:TX), teste=EXT_TR_SWb 1: RXDATA, Test1, testse back to previous define.
6	reserved	
5	LNA_TST_PD	When "1", indicate to power down LNA during AMS_TST_ENB = "1".
4	ADC_TST_PD	When "1", indicate to power down ADC during AMS_TST_ENB = "1".
3	RF_VCO_TST_PD	When "1" is given, indicate to power down the RF VCO circuits during AMS_TST_ENB = "1".
2	RC_TST_START	Provide test value for RC START during AMS_TST_ENB = "1".
1	RC_TST_PD	When "1", indicate to power down RC circuit during AMS_TST_ENB = "1".
0	MIXER_TST_PD	When "1", indicate to power down mixer during AMS_TST_ENB = "1".

Introduction of JF24C register setting

TX/RX Data Control (Write/Read) – Register 18 (Default 0xE000)

Bit No.	Bit Name	Description
15	SOFTWARE_CNTL	Set this bit to enable software to control the assertion time of PA_ON and SW_ON based on the values of TX_PA_ON_DELAY and TX_SW_ON_DELAY respectively; default setting '0' is to select HW state machine to control those timing.
14	RX_DATA_INVERSE	The control signal provides the convenience for using the upper band or lower band of IF signal. When "1" is given, the polarity of the received signals BDATA1 or RXDATA will be inverse.
13	BYPASS_PLL_LOCK	When "1" is given, the transmitter will start to put the data on the air just after the time out of TX delay, and will not wait for the stable state of RF PLL.
12 – 10	TX_CW[2:0]	Set the time period to transmit CW bits in TX mode after TR_SW is on; when this time period expires, TX data from BB will be transmitted.
9	BRCLK_SW	"1" : route the 12M from APLL to BRCLK pin.
8	TX_DATA_INVERSE	When "1" is given, the polarity of the transmitting data BDATA1 will be inverse internally.
7-0	Reserved	

Introduction of JF24C register setting

DC Offset Control (Write/Read) – Register 19 (Default 0x2114)

Bit No.	Bit Name	Description
15	LNA_HP	LNA high power
14	LOBUF_HP	PA high power
13	ADC_LP	ADC low power
12	reserved	
11-9	Reserved	
8	Bpktctl_sel	1: BPKTCTL control wide mode to Narrow mode in receiving
7-4	WIDE_TC[3:0]	Select the time period for DC offset wide mode; during this period, DC offset circuit will use the speed set by bit 3-2 to track DC offset values; after selected time period expires DC offset circuit will automatically switch to the speed of narrow mode (bit 1-0 of this register). Please note the tracking speed in wide mode will be always faster than in narrow mode.
3-2	WIDE_TRACK_SPEED[1:0]	Set alpha value for DC offset tracking speed in RX wide mode.
1-0	NARROW_TRACK_SPEED[1:0]	Set alpha value for DC offset tracking speed in RX narrow mode.

Introduction of JF24C register setting

PLL/VCO Control (Write/Read) – Register 20 (Default 0x819C)

Bit No.	Bit Name	Description
15	PLL_FREQ_PLUS	Set to choose the upper sideband Low IF signal or lower sideband Low IF signal to be demodulated
14 – 8	PLL_RX_FREQ_OFFSET	Set the RF PLL offset frequency above local oscillator.
7 – 5	A_INIT[2:0]	PLL A count initial value in power down mode
4	SYNTH_LP	Set PLL low power
3	LNA_LP	Set LNA low power
2	LOBUF_LP	Set local soc buffer low power
1--0	RSSI_R	

PLL Synthesizer Control (Write/Read) – Register 21 (Default 0x6962)

Bit No.	Bit Name	Description
15	APLL_IDLE_OFF	1: APLL will be put into the power-off state in IDLE.
14	RF_VCO_IDLE_OFF	The RF VCO will be put into the power-off state if SYNTH_IDLE_OFF is “HIGH”; otherwise, they will be still active when SYNTH_IDLE_OFF is “LOW”.
13	SYNTH_IDLE_OFF	The Synthesizer will be put into the power-off state if SYNTH_IDLE_OFF is “HIGH”; otherwise, they will be still active when SYNTH_IDLE_OFF is“LOW”.
12	RF_PLL_DIRECT	When the RF_PLL_DIRECT is set to “1”, the synthesizer will be programmed directly with Register7[11:0]. The frequency of synthesizer will not be programmed as f = 2402+ PLL_CH_NO again.
11 – 0	PLL_RF_FREQ_BASE	Set the RF PLL base frequency.(Default = 2402 MHz)

Introduction of JF24C register setting

CONFIGURE_REG Register 48 (default 0x5800):config

Bit	Name	R/W	Description
15:13	Preamble_len	R/W	000: 1byte, 001: 2bytes, 010: 3 bytes, . 111: 8 bytes Note: in transmit mode, always keep 8bit "1010…" before BPKTCTL as sync data
12:11	Syncword_len	R/W	11: 64 bits, {Reg55[15:0],Reg54[15:0],Reg53[15:0],Reg52[15:0]} 10: 48bits, {Reg55[15:0],Reg54[15:0],Reg52[15:0]} 01: 32bits, {Reg55[15:0],Reg52[15:0] 00: 16 bits,{Reg52[15:0]}
10:8	Trailer_len	R/W	000: 4 bits, 001: 6bits, 010: 8 bits, 011: 10 bits . 111: 18bits
7:6	Data packet type	R/W	00: NRZ law data 01: Manchester data type 10: 8/10 line code 11: interleave date type
5:4	FEC type	R/W	00: No FEC 01: FEC13 10: FEC23 11: reserved
3	Power done	W	1: framer set BnPWR low to RFIC, than off the crystal buffer
2	Sleep mode	W	1: framer set BXTLEN low to RFIC, then off the crystal
1	Reset RFIC	W	1: MCU just to reset RFIC, once short
0	Fun_sel	W	1: framer off. 0: framer on

Introduction of JF24C register setting

SYNC_WORD_1 Register 5. *(default 0x0000)*

Bit	Name	Description
15:0	SYNC_WORD[15:0]	LSB bits of sync word is first, it match the BT SPEC.? In different syncword length, this register is first send out.

SYNC_WORD_2 Register 53 *(default 0x0000)*

Bit	Name	Description
15:0	SYNC_WORD[31:16]	LSB bits of sync word is first

SYNC_WORD_3 Register 5. *(default 0x0000)*

Bit	Name	Description
15:0	SYNC_WORD[47:32]	LSB bits of sync word is first

SYNC_WORD_4 Register 55 *(default 0x0000)*

Bit	Name	Description
15:0	SYNC_WORD[63:48]	LSB bits of sync word is first

Introduction of JF24C register setting

Threshold_reg Register 56 *(default 0x4407)*

Bit	Name	Description
15:12	TX_FIFO_threshold	
11:8	RX_FIFO_threshold	
7	Pkt_hint_pority	1: PKF_flag/FIFO_flag low active. 0: high active
6	addr_match_opt	Addr_match time option to fix RXCLK gitter
5:0	Syncword_threshold	

RF_CTRL Register 57 *(default 0xB000)*

Bit	Name	Description
15	CRC_on	0: CRC off. 1: CRC on
14	Scramble_on	0: scramble off. 1: scramble on
13	Pack_lenth_en	1: HW regards first byte payload is length
12	DIRECT_COTROL_MASK	1: RF status from off status to idle status is controlled by BNPWR_PIN,BXTLEN_PIN,BDATA1_PIN. 0: When RESET_n = 1, waiting certain timing, RF status will be automatically enter idle status.
11	BNPWR_PIN	
10	BXTLEN_PIN	
9	BDATA1_PIN	
8	Fw_term_tx	0:FW handle packet length and terminate TX by FW 1:when FIFO write point equals read point, HW terminate TX when FW handle packet length
7:0	CRC initial data	

Introduction of JF24C register setting

Main_status Register 64 ***(Read only)***

Bit	Name	Description
15:12	Framer/RFIC_st	BnPWR, BXTLEN, TX_EN, RX_EN 0xxx: OFF status 1000: sleep staus 1100: Idle 1110: transmit 1101: receive others: illegal status
11	Error_ok	1: have error in receiving Include FEC | CRC check, it will be cleared in next start RX/TX
10	Syncword_rev	1: syncword received, it is just available in receive status, after out receive status, always keep '0'
9:8	Reserved	
7:4	Framer TX status	Come from HW TX state machine, also can help HW to debug
3:0	Framer RX status	Come from HW RX state machine.

Introduction of JF24C register setting

TX_FIFO_REG Register 80

Bit	Name	Description
15:0	TXRX_FIFO_REG	For MCU read/write data between the FIFO

FIFO_RD_PTR Register 82

Bit	Name	Description
15	Clr_w_ptr	1: clear TX FIFO point to 0 when write this bit to “1”. It is not available in RX status
14:8	FIFO_WR_PTR	FIFO write point
7	Clr_r_ptr	1: clear RX FIFO point to 0 when write this bit to “1”. It is not available in TX status
6:0	FIFO_RD_PTR	FIFO read point

Recommended register setting

RF initialization

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x09	R/W	3003	2001
0x00	R/W	CD51	354D
0x02	R/W	137B	1F01
0x04	R/W	3CD0	BCF0
0x05	R/W	0081	00A1
0x07	R/W	0030	124C
0x08	R/W	0404	8000
0x0C	R/W	0000	8000
0x0E	R/W	6697	169B
0x0F	R/W	017B	90AD
0x10	R/W	F000	B000
0x13	R/W	2114	A114
0x14	R/W	819C	8191
0x16	R/W	0402	0002
0x18	R/W	B040	B140
0x19	R/W	7819	A80F
0x1A	R/W	6704	3F04
0x1C	R/W	1800	5800

Recommended register setting

Framer initialization

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0x30	R/W	5800	9800
0x31	R/W	C00F	FF8F
0x32	R/W	9628	8028
0x33	R/W	8300	8056
0x34	R/W	0000	4EF6
0x35	R/W	0000	F6F5
0x36	R/W	0000	185C
0x37	R/W	0000	D651
0x38	R/W	4407	4444
0x39	R/W	B000	E000

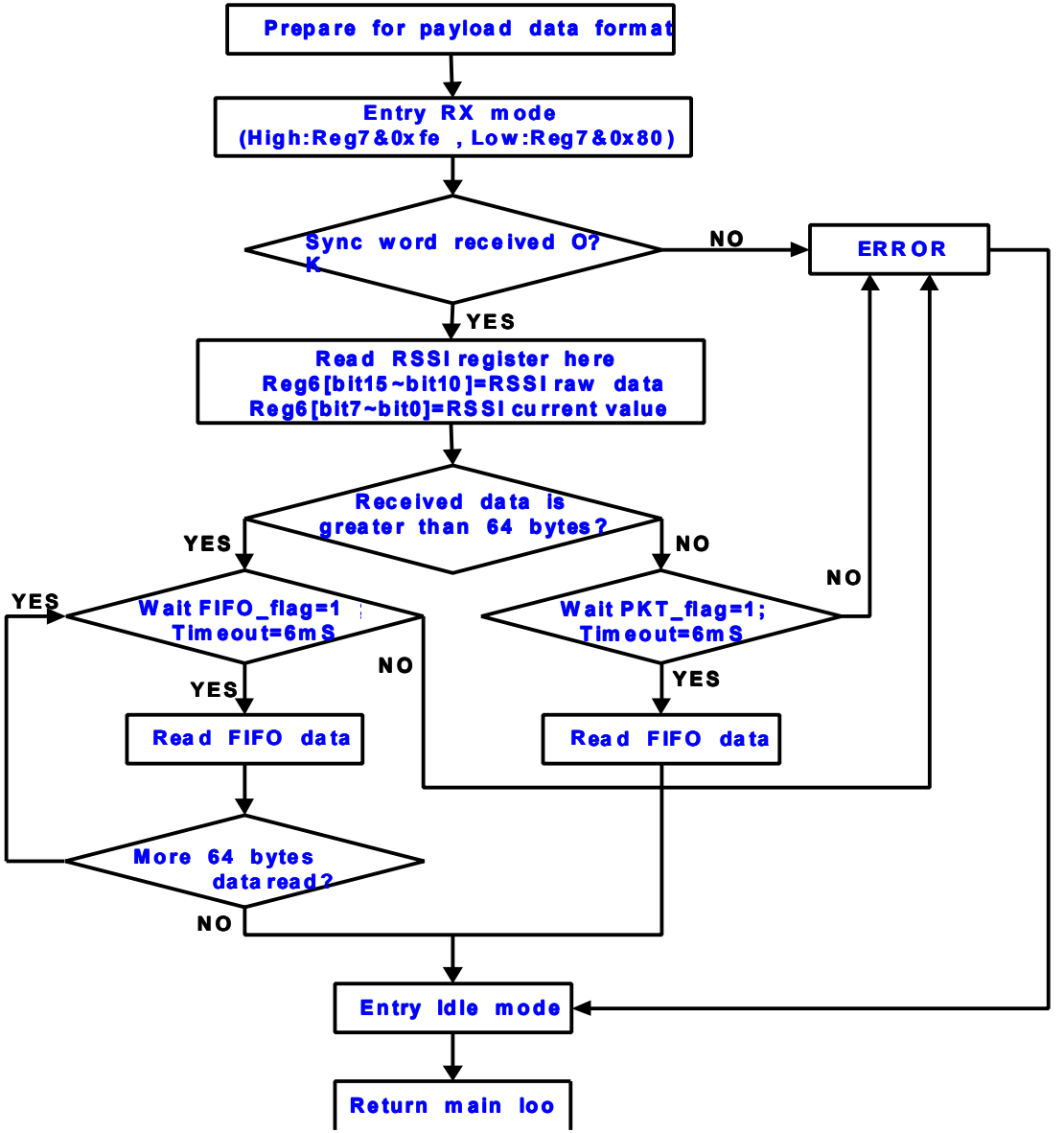
Reg57, if MCU handle packet length and framer detect FIFO fully empty, Reg57=0xC080

Reg57, if MCU handle packet length and terminates TX done, Reg57=0xC000

Reg. address	Read/Write	Default value (Hexadecimal)	Recommend value (12MHz crystal frequency) (Hexadecimal)
0	R/W	0000	CD51
2	R/W	00C1	0061
4	R/W	0688	3CD0
5	R/W	0041	00A1
9	R/W	0003	3003
14	R/W	6617	6697
16	R/W	0000	F000
18	R/W	FC00	E000
19	R/W	0014	2114
20	R/W	8103	819C
21	R/W	0962	6962
22	R/W	2602	0402
23	R/W	2602	0802
24	R/W	30C0	B080
25	R/W	3814	7819
26	R/W	5304	6704
48	R/W	1800	5800
51	R/W	4000	A000
56	R/W	4407	4407
57	R/W	B000	E000*

How to read RSSI value from JF24C?

For reading RSSI value flow chart:



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